

5-WIDE 5, 4, 4, 4, 2 OA/OAI GATE

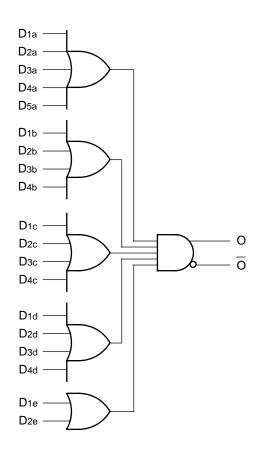
FEATURES

- Max. propagation delay of 800ps
- IEE min. of –55mA
- Extended supply voltage option: VEE = -4.2V to -5.5V
- Voltage and temperature compensation for improved noise immunity
- Internal 75kΩ input pull-down resistors
- 70% faster than Fairchild
- 40% lower power than Fairchild
- Function and pinout compatible with Fairchild F100K
- Available in 28-pin PLCC package

DESCRIPTION

The SY100S318 is an ultra-fast 5-wide 5, 4, 4, 4, 2 OR/ AND gate with both true and complementary outputs, designed for use in high-performance ECL systems. The inputs on this device have $75k\Omega$ pull-down resistors.

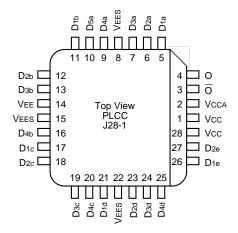
BLOCK DIAGRAM



PIN NAMES

Pin	Function					
Dna – Dne	Data Inputs (n = 15)					
0-0	Data Outputs					
VEES	VEE Substrate					
VCCA	Vcco for ECL Outputs					

PACKAGE/ORDERING INFORMATION



Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY100S318JC	J28-1	Commercial	SY100S318JC	Sn-Pb
SY100S318JCTR ⁽¹⁾	J28-1	Commercial	SY100S318JC	Sn-Pb
SY100S318JZ ⁽²⁾	J28-1	Commercial	SY100S318JZ with Pb-Free bar-line indicator	Matte-Sn
SY100S318JZTR ^(1, 2)	J28-1	Commercial	SY100S318JZ with Pb-Free bar-line indicator	Matte-Sn

Notes:

1. Tape and Reel.

2. Pb-Free package is recommended for new designs.

28-Pin PLCC (J28-1)

LOGIC EQUATION

O = (D1a + D2a + D3a + D4a + D5a)(D1b + D2b + D3b + D4b) (D1c + D2c + D3c + D4c) (D1d + D2d + D3d + D4d) (D1e + D2e)

DC ELECTRICAL CHARACTERISTICS

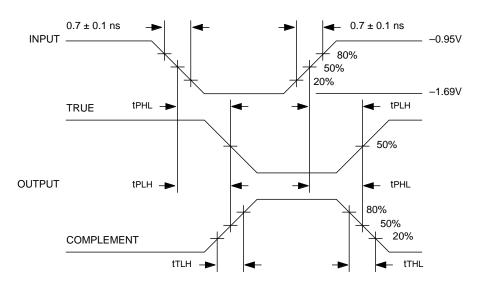
VEE = $-4.2V$ to $-5.5V$ unless otherwise specified, VCC = VCCA = GND							
Symbol	Symbol Parameter		Тур.	Max.	Unit	Condition	
Іін	Input HIGH Current, All Inputs	—		200	μΑ	VIN = VIH (Max.)	
IEE	Power Supply Current	-55	-41	-25	mA	Inputs Open	

AC ELECTRICAL CHARACTERISTICS

VEE = -4.2V to -5.5V unless otherwise specified, VCC = VCCA = GND

		TA = 0°C		TA = +25°C		TA = +85°C			
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit	Condition
tPLH tPHL	Propagation Delay Data to Output	300	800	300	800	300	800	ps	
tтlн tтнl	Transition Time 20% to 80%, 80% to 20%	200	900	200	900	200	900	ps	

TIMING DIAGRAM

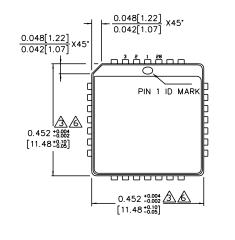


Propagation Delay and Transition Times

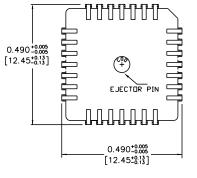
Note:

VEE = -4.2V to -5.5V unless otherwise specified, Vcc = Vcca = GND

28-PIN PLCC (J28-1)



TOP VIEW

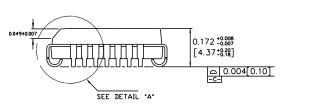


BOTTOM VIEW

0.020[0.51] MÍN.

1

0.050[1.27] BSC



SIDE VIEW

NOTES:

- 1.
- TILS: DIMENSIONS ARE IN INCHES [MM]. CONTROLLING DIMENSION: INCHES. DIMENSION DOES NOT INCLUDE MOLD FLASH OR PROTRUSIONS, EITHER OF WHICH SHALL NOT EXCEED 0.008 [0.203]. LEAD DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. A
- <u>A</u>
- MAXIMUM AND MINIMUM SPECIFICATIONS ARE INDICATED AS FOLLOWS: MAX/MIN 5.
- \mathbb{A} PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.



0.021 [0.53] 0.013 [0.33]

0.032[0.81] 0.026[0.66]

Rev. A

 $\begin{smallmatrix} 0.0100 & \stackrel{+0.0003}{-0.0003} \\ [0.254 & \stackrel{+0.008}{-0.008}] \\ \end{smallmatrix}$

0.101 +0.019

 $[2.56^{+0.49}_{-0.27}]$

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